IN THE CLAIMS

We claim:

1. An apparatus comprising:

a first addressable device associated with a first device identifier (ID);

a second addressable device stacked adjacent the first addressable device, wherein the second addressable device is coupled to the first addressable device and includes a circuit to generate a second device ID as a function of the first device ID.

2. The apparatus of Claim 1, wherein the first addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

3. The apparatus of Claim 1, wherein the second addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

4. The apparatus of Claim 1, wherein the first device ID is encoded.

5. The apparatus of Claim 1, wherein the circuit is a +N adder circuit.

6. The apparatus of Claim 1, wherein the circuit is selected from the group including a –N adder circuit, a combinatorial logic circuit, an active logical shifter, and a passive logical shifter.

7. An apparatus comprising:

a first addressable device having a first device ID;

a second addressable device stacked on the first addressable device, wherein the second addressable device is coupled to the first addressable device and includes means for generating a second device ID as a function of the first device ID.

8. The apparatus of Claim 7, wherein the first addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

9. The apparatus of Claim 7, wherein the second addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

10. The apparatus of Claim 7, wherein the first device ID is encoded.

11. An apparatus comprising:

a first integrated circuit die and a second integrated circuit die in a stacked configuration, the first integrated circuit die including:

a through-silicon via; and

a device identification (ID) generating circuit, the device ID generating circuit to receive a first device ID and to provide a second, different device ID that is a function of the first device ID, the second device ID to identify the second integrated circuit die.

12. A method comprising:

stacking a plurality of addressable devices in a package, the package having a package substrate;

encoding a device ID for one addressable device in the stack; and

determining the device ID for each of the plurality of addressable devices whose device ID is not encoded based upon the device ID of an adjacent device in the stack.

13. The method of Claim 12, wherein the plurality of addressable devices are selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

14. The method of Claim 12, wherein the device ID for one addressable device in the stack is encoded in the package substrate.

15. The method of Claim 12, further comprising electrically coupling the package to a printed circuit board.

16. The method of Claim 15, wherein the device ID for one addressable device in the stack is encoded in the printed circuit board.

17. The method of Claim 12, further comprising bonding the plurality of stacked addressable devices to each other using through-silicon via technology.

18. The method of Claim 12, further comprising coupling the plurality of stacked addressable devices to each other optically.

19. The method of Claim 12, further comprising capacitively coupling the plurality of stacked addressable devices to each other.

20. The method of Claim 12, wherein each of the plurality of addressable devices whose device ID is not encoded contains a +N adder circuit.

21. The method of Claim 12, wherein each of the plurality of addressable devices whose device ID is not encoded contains a -N adder circuit.

22. The method of Claim 12, wherein each of the plurality of addressable devices whose device ID is not encoded contains combinatorial logic to produce a desired output from a given input.

23. The method of Claim 12, wherein each of the plurality of addressable devices whose device ID is not encoded contains an active logical shifter.

24. The method of Claim 12, wherein each of the plurality of addressable devices whose device ID in the printed circuit board contains a passive logical shifter.

25. The method of Claim 12, wherein the device ID determined for each of the plurality of addressable devices is unique to one of the plurality of addressable devices.

26. A method comprising:

stacking a plurality of addressable devices;

coupling each of the plurality of addressable devices to the device below it and the device above it;

encoding a device ID for one of the plurality of addressable devices; and

determining the device ID for each of the plurality of addressable devices whose device ID is not encoded based upon the device ID of an adjacent device in the stack.

27. The method of Claim 26, wherein the plurality of addressable devices are selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

28. The method of Claim 26, wherein the plurality of addressable devices are coupled electrically.

29. The method of Claim 26, wherein the plurality of addressable devices are coupled optically.

30. The method of Claim 26, wherein the plurality of addressable devices are coupled capacitively.

31. The method of Claim 26, wherein each of the plurality of addressable devices whose device ID is not encoded contains a +N adder circuit.

32. The method of Claim 26, wherein the device ID determined for each of the plurality of addressable devices is unique to one of the plurality of addressable devices.

33. The method of Claim 26, further comprising coupling one of the plurality of addressable devices to a printed circuit board.

34. The method of Claim 33, wherein the device ID for one addressable device in the stack is encoded in the printed circuit board.

35. The method of Claim 26, wherein the device ID for one addressable device in the stack is electrically encoded in non-volatile memory within the one addressable device.

36. The method of Claim 26, wherein the device ID for one addressable device in the stack is electrically encoded in fuses within the one addressable device

37. The method of Claim 26, wherein the device ID for one addressable device in the stack is hard-wired within the one addressable device using a metal option.

38. A system comprising:

a bus;

a processor coupled to the bus;

a first addressable device coupled to the bus and having a first device ID;

a second addressable device stacked on the first addressable device, wherein the second addressable device is coupled to the bus and coupled to the first addressable device, and includes a circuit to generate a second device ID as a function of the first device ID; and

an RF interface coupled to the processor.

39. The system of Claim 38, wherein the first addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

40. The system of Claim 38, wherein the second addressable device is selected from the group including flash memory, SRAM, DRAM, SDRAM, EPROM, EEPROM, ROM, MEMS devices, MEMS memory, and memory plus logic devices.

41. The system of Claim 38, wherein the first device ID is encoded.

42. The system of Claim 38, wherein the circuit is a +N adder circuit.

43. The system of Claim 38, wherein the circuit is selected from the group including a –N adder circuit, a combinatorial logic circuit, an active logical shifter, and a passive logical shifter.